# Capacitor with Enhanced Performance and Method of Manufacture

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application relates to co-pending and commonly assigned patent application Serial No. _____, filed concurrently herewith and entitled "Capacitor with Improved Capacitance Density and Method of Manufacture" (TSM-03-0555), which application is hereby incorporated herein by reference.

## TECHNICAL FIELD

**[0002]** The present invention relates generally to semiconductor devices and more particularly to a capacitor with enhanced performance and method of manufacture.

## BACKGROUND

**[0003]** Power supply lines in a semiconductor integrated circuit chip supply current to charge and discharge active and passive devices in the integrated circuit. For example, digital complementary metal-oxide-semiconductor (CMOS) circuits draw current when the clock makes a transition. During the operation of circuits, the power supply lines must supply transient currents with a relatively high intensity, and can result in voltage noise on the power supply lines. The voltage on the power supply line will fluctuate when the fluctuation time of the transient current is short or when its parasitic inductance or parasitic resistance is large.

**[0004]** In state-of-the-art circuits, the operational frequency of the integrated circuit is in the order of several hundreds of mega-hertz (MHz) to several giga-hertz (GHz). In such circuits, the rising time of clock signals is very short, so that voltage fluctuations in the supply line can be very large. Undesired voltage fluctuations in the power supply line powering a circuit can cause

noise on its internal signals and degrade noise margins. The degradation of noise margins can reduce circuit reliability or even cause circuit malfunction.

**[0005]** To reduce the magnitude of voltage fluctuations in the power supply lines, filtering or decoupling capacitors are usually used between the terminals of different power supply lines or between terminals of power supply line and the ground line. Decoupling capacitors act as charge reservoirs that additionally supply currents to circuits when required to prevent momentary drops in supply voltage.

**[0006]** Figure 1 shows a circuit diagram containing these decoupling capacitors. Capacitor $C_1$ is a decoupling capacitor that is inserted between a power supply line $V_{DD}$ and the ground line *GND*. Most chips employ more than one power supply line, and may have a different power supply line $OV_{DD}$ for the output circuits that interface with external circuits. Capacitor $C_2$ is a decoupling capacitor that is inserted between the output voltage supply line $OV_{DD}$ and the ground line *GND*. Capacitor $C_3$ is a decoupling capacitor that is inserted between the supply line $V_{DD}$ and the output voltage supply line $OV_{DD}$. These decoupling capacitors are usually placed as close as possible to the transient current source or sink.

**[0007]** Decoupling capacitors are used in integrated chips employing both bulk and silicon-on-insulator substrates. However, the role of decoupling capacitors is more important in a silicon-on-insulator chip than in a bulk silicon chip due to the following reason. Integrated chips fabricated on bulk substrates can naturally decouple the power supply potential and the ground potential due to the presence of inherent depletion capacitances between the doped wells and the bulk substrate. Compared to bulk substrates, silicon-on-insulator chips have very low on-chip decoupling capacitance between the power supply lines and ground.

**[0008]** U.S. Patent No. 6,558,998 entitled "SOI type integrated circuit with a decoupling capacity and process for embodiment of such a circuit" issued to Belleville *et al.* describes a decoupling capacitor that is formed with the formation of silicon-on-insulator substrates. While that capacitor may be formed with a large area or large capacitance, it is formed together with the substrate, which means that the substrate has to be customized for each different circuit design.

## SUMMARY OF THE INVENTION

**[0009]** These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention which teach an integrated circuit capacitor with enhanced performance and method of manufacture a capacitor.

**[0010]** In accordance with a preferred embodiment of the present invention, a capacitor is formed in a strained semiconductor layer. In particular, a bottom electrode is formed in a portion of the strained semiconductor layer. A capacitor dielectric overlies the bottom electrode and a top electrode overlies the capacitor dielectric. In one embodiment, first and second bottom electrode contact regions are formed in the strained semiconductor layer adjacent but not underlying the top electrode. The bottom electrode is located between the first and the second bottom electrode contact regions. In this embodiment, the first bottom electrode region is electrically coupled to the second bottom electrode region, e.g., by at least one metallization layer.

**[0011]** In a second embodiment of the present invention, a decoupling capacitor is formed in a semiconductor substrate that includes a strained silicon layer. A substantially flat bottom electrode is formed in a portion of the strained silicon layer and a capacitor dielectric overlying the bottom electrode. A substantially flat top electrode overlies said capacitor dielectric. The top electrode is connected to a first reference voltage line and the bottom electrode is connected to a second reference voltage line.

**[0012]** The present invention also teaches a method of forming a capacitor. A semiconductor substrate that includes a strained silicon layer is provided. A bottom electrode is

formed in the strained silicon layer, e.g., by doping the layer. A capacitor dielectric is formed on bottom electrode and a top electrode is formed on capacitor dielectric. A first doped region and a second doped region are formed within the strained silicon layer adjacent but not beneath the top electrode. These doped regions are electrically connected to each other. Alternatively, only one doped region may be used to electrically contact the bottom electrode.

**[0013]** The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

**[0015]** Figure 1 shows an equivalent circuit of known decoupling capacitors;

**[0016]** Figure 2 shows a capacitor of a first embodiment of the present invention;

**[0017]** Figures 3a-3e provide diagrams to illustrate the concept of a strained layer;

**[0018]** Figure 4 provides a circuit model or equivalent circuit of a capacitor employing an inversion layer as a bottom electrode;

**[0019]** Figure 5 shows an energy band diagram illustrating the direct tunneling current through the capacitor dielectric;

**[0020]** Figure 6 shows a capacitor of a second embodiment of the present invention;

**[0021]** Figure 7 shows a top view or layout of a capacitor of the present invention;

**[0022]** Figures 8a and 8b show cross sectional views of the capacitor of Figure 7;

**[0023]** Figures 9a and 9b show cross sectional views of another embodiment capacitor; and

**[0024]** Figures 10a-10f show cross sectional views of a capacitor of the present invention during various stages of the fabrication process.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

**[0025]** The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

**[0026]** In the preferred embodiment this invention, a capacitor structure with at least one strained electrode is taught. The strained electrode may, for example, be comprised of a strained silicon layer. For example, the strained electrode can be a heavily doped strained silicon layer or it can be an inversion layer in a strained silicon layer.

**[0027]** Figure 2 shows a specific embodiment of this invention. Figure 2 shows a semiconductor substrate 102 with a top strained silicon layer 104. A capacitor 100 is formed on substrate 102 and includes top electrode 106 that overlies a capacitor dielectric 108. The bottom electrode of the capacitor is the inversion layer formed in the strained silicon layer 104. One or more doped regions 110 (and 112) are formed adjacent to the inversion layer to electrically contact an inversion layer 114. The capacitor 100 may be isolated from other devices of the semiconductor chip by trench isolation regions 116, for example. The strained silicon region can be formed in a well 124, which may be part of substrate 102.

**[0028]** In the embodiment of Figure 2, the capacitor is formed from the top electrode 106 and the bottom electrode 104. The top electrode can easily be contacted to since an upper surface is exposed. To contact the bottom electrode, bottom electrode contact regions 110 and/or

112 are provided. In one embodiment, the bottom electrode 104 is doped to the same conductivity type as the contact regions 110 and 112.

**[0029]** In another embodiment, the bottom electrode 104 is doped to a different conductivity type. In this case, the inversion region 114 is provided to create the contact between regions 104, 110 and 112. For example, in one embodiment the contact regions 110 and 112 are physically doped with n-type dopants (e.g., arsenic and/or phosphorus) and the electrode region 104 is physically doped with p-type dopants (e.g., boron). When the top electrode is connected to a high voltage level, inversion region 114 will be formed and will appear to be n-doped. In this manner, the bottom electrode contact regions 110 and/or 112 are doped to a given conductivity type (n-type in this example) and the bottom electrode is operationally doped the first conductivity type. In this context, "operationally doped" means being at that doping level whenever the chip is operational. This definition excludes a transistor, which is at that doping level only when that transistor itself is turned on.

**[0030]** Figures 3a-3e show an example of how a strained layer may be formed. In the preferred embodiment, the strained layer 104 is strained silicon. As shown in Figure 3a, the strained silicon 104 is formed on a semiconductor 118 with a lattice constant that is larger than the relaxed lattice constant of silicon, e.g., relaxed silicon-germanium (SiGe) layer. The relaxed SiGe layer 118 may overlie a graded SiGe buffer layer 120, which is grown on a silicon substrate 122. The relaxed SiGe layer 118 can be thought of as a stressor that introduces strain in the silicon layer 104. The stressor, in this case, is placed below the strained silicon layer 104.

**[0031]** Figures 3b and 3c illustrate the effect of the relaxed SiGe layer 118 on a pseudomorphically strained silicon layer 104. Figure 3b shows that the two semiconductors have different lattice constants in the natural state and Figure 3c shows the strain created in the silicon

layer 104 when the two layers 104 and 118 are joined. The strained silicon 104 may be under biaxial tension. Significant mobility enhancement has been reported for both electrons and holes in silicon under biaxial tensile strain.

**[0032]** The mobility enhancement can be explained as follows. In relaxed silicon, the electrons reside in the six-fold degenerate $\Delta_6$ conduction valleys as illustrated by Figure 3d. With the introduction of biaxial tension in silicon, the conduction valleys split into two energy levels as shown in Figure 3e. The two-fold degenerate valleys labeled $\Delta_2$ has a lower energy and higher in-plane mobility than the four-fold degenerate valleys labeled $\Delta_4$. The difference in energy between the $\Delta_2$ and $\Delta_4$ levels is $\Delta E$. For strained silicon grown on a relaxed $Si_{1-x}Ge_x$ buffer layer, the value of $\Delta E$ is given by 0.67x (in eV). Since most of the electrons reside in the two-fold degenerate valleys, the average electron mobility is significantly improved.

**[0033]** According to the preferred embodiment of this invention, a heavily doped strained silicon layer or an inversion region in a strained silicon layer is used as a bottom electrode of a capacitor. The heavily doped strained silicon is preferably heavily doped with n-type dopants, and the inversion region preferably comprises electrons because the mobility of electrons is significantly increased in strained silicon. The resistance of the inversion region is inversely proportional to mobility. A high mobility inversion region has a lower resistance. Therefore, by forming a low resistance inversion layer in the strained silicon layer, and employing it as a bottom electrode of a capacitor, the capacitor is formed with an electrode with significantly improved conductance. The capacitor may be used as a decoupling capacitor in the preferred embodiment, but it is understood that the capacitor thus formed may be used for other analog or digital applications.

**[0034]** Referring now to Figure 4, a circuit model or equivalent circuit of the capacitor 100 is shown. In Figure 4, the top electrode 106 of the capacitor is depicted using a horizontal bar and connected to a node labeled G. The capacitor dielectric 108 is modeled using a distributed equivalent circuit approach, with a normalized tunneling impedance of the capacitor dielectric $r_t$, and a normalized capacitance density c. A capacitor dielectric with a low leakage has a high $r_t$. Therefore, a large $r_t$ is desired.

**[0035]** On the other hand, the sheet resistance $r_s$ of the inversion layer 114 should be as small as possible. Since the inversion layer 114 electrically communicates with adjacent doped regions 110 and 112, also known as the source and drain regions, the sheet resistances are connected to nodes 110 and 112 at the two ends of the circuit diagram of Figure 4. The inversion layer 114 is electrically connected to the well region 124 through body resistances $r_b$. The well region 124 is typically connected to a ground potential. The value of $r_b$ is typically large since no significant current flow between the inversion layer and the well region. In addition, since there is no net current flow across the center of the capacitor, each half of the circuit sees an open circuit termination.

**[0036]** The improvement to the sheet resistance of the inversion channel $r_s$ is one of the advantages of the preferred embodiment of this invention. According to this embodiment, by forming the inversion layer in a strained silicon layer and using it as a bottom electrode, the value of $r_s$ is smaller than that in a conventional relaxed silicon channel. A smaller value of $r_s$ contributes to a smaller series resistance in the capacitor, or a smaller resistance in one of the electrodes of the capacitor. A smaller electrode resistance leads to a lower equivalent series resistance (ESR). The ESR is defined to be the impedance or resistance of the capacitor at its resonant frequency. A low ESR is one of the desirable characteristics for a decoupling capacitor

used in high frequency circuits. In high frequency circuits, it is advantageous to employ decoupling capacitors with low total impedance of resistance over a wide frequency range.

**[0037]** Another benefit of the preferred embodiment of this invention is the reduction of leakage current through the capacitor dielectric 108. Referring now to Figure 5, an energy band diagram is drawn to show the conduction band along the line A-A' in the capacitor structure of Figure 2. The line A-A' passes from the top electrode 106 to the capacitor dielectric 108 to the strained silicon layer 104 and the semiconductor substrate 102. The semiconductor substrate 102 is taken to be SiGe, for example.

**[0038]** An electron (depicted by a circle labeled 126) in the strained silicon layer 104 will see a barrier height given by $\Phi_b$ as indicated in Figure 5. This electron may be in an inversion layer in the strained silicon 104, or this electron may be a mobile carrier in a heavily doped strained silicon layer. The quantum mechanical tunneling of the electron through the capacitor dielectric 108 to the top electrode 106 contributes to a tunneling leakage current, which is undesirable. Due to the splitting of the energy levels in the conduction band of the strained silicon layer, the bottom-most $\Delta_2$ level in the strained silicon layer has a reduced or lower energy level compared to the $\Delta_6$ level in a relaxed silicon layer. As a result of the reduced energy level in the conduction band of the strained silicon, the barrier height seen by the electron will be larger. The larger barrier height results in a reduced tunneling probability and therefore a reduced leakage current. Therefore, a capacitor structure employing strained silicon as the bottom electrode gives a lower leakage current compared to one using relaxed silicon as the bottom electrode.

**[0039]** Figure 6 shows another embodiment of the present invention where the strained silicon 104 is formed not on a relaxed silicon germanium buffer layer, but on an insulator layer

130. Such a substrate 132 is also known as a strained-silicon-on-insulator (SSOI) substrate, and comprises a strained silicon layer 104 overlying an insulator layer130, which in turn overlies a semiconductor substrate 132. Another semiconductor layer (not shown), such as a SiGe layer, may or may not be inserted between the strained silicon layer 104 and the insulator layer 130.

**[0040]** Such a substrate 132 may be formed by a layer transfer technique, such as by the transfer of a strained silicon layer onto a target wafer with an insulator surface. The bottom electrode 104 may be lightly doped and electrically contacted by a highly doped region, or the bottom electrode 104 may be a high-doped region.

**[0041]** In Figure 6, the capacitor is isolated from other circuit elements by trench isolation 116, but it is understood that other forms of isolation, for example, mesa isolation may be used. In mesa isolation, trenches are not filled with a dielectric filling material prior to the formation of transistors or capacitors. In a semiconductor chip employing mesa isolation, trenches between active regions are not filled with dielectric prior to the formation of active devices.

**[0042]** According to embodiments of this invention, the capacitor dielectric 104 can be any dielectric. For example, the capacitor dielectric can be conventional gate dielectrics known and used in the art, e.g. silicon oxide, silicon oxynitride, or silicon nitride, or combinations thereof. In another embodiment, the capacitor dielectric may be comprised of a high permittivity (high-k) dielectric. By using a high-k dielectric as the capacitor dielectric, the capacitance density $\frac{\varepsilon_0 \varepsilon_r}{t_{phys}}$ is significantly higher than that of a capacitor employing a conventional silicon oxide dielectric, where $\varepsilon_0$ is the permittivity of free space, $\varepsilon_r$ is the relative permittivity, and $t_{phys}$ is the physical thickness of the capacitor dielectric.

**[0043]** The high-k dielectric preferably has a permittivity of larger than about 5, and more preferably has a permittivity of larger than about 10, and even more preferably has a permittivity of larger than about 20. The high permittivity dielectric may be selected from a group comprising of aluminum oxide ($Al_2O_3$), hafnium oxide ($HfO_2$), hafnium oxynitride (HfON), hafnium silicate ($HfSiO_4$), zirconium oxide ($ZrO_2$), zirconium oxynitride (ZrON), zirconium silicate ($ZrSiO_4$), or combinations thereof. In the preferred embodiment, the high-k dielectric is hafnium oxide. The silicon oxide equivalent thickness (EOT) of the capacitor dielectric is preferably smaller than about 100 angstroms, more preferably smaller than about 50 angstroms, and even more preferably smaller than about 10 angstroms. The physical thickness of the capacitor dielectric may be smaller than about 100 angstroms, more preferably smaller than about 50 angstroms, and even more preferably smaller than about 10 angstroms.

**[0044]** The top electrode 106 comprises a conductive material such as poly-crystalline silicon, poly-crystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, or a metallic oxide, or combinations thereof. Metals such as molybdenum, tungsten, titanium, tantalum, platinum, and hafnium may be used as the portion of the top electrode 106. Metallic nitrides may include, but are not limited to, molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride. Metallic silicides may include, but are not limited to, nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide. Metallic oxides may include, but are not limited to, ruthenium oxide and indium tin oxide.

**[0045]** The decoupling capacitor 100 may be formed in an active region in the vicinity of an active device such as a transistor (not shown). The capacitor dielectric may comprise the same dielectric as the transistor gate dielectric.

**[0046]** Figure 7 is a top view or layout view of the capacitor 100 of the preferred embodiment of this invention. The capacitor 100 has a width W and a length L. In the preferred embodiment, the width W may have a dimension of larger than about 5 microns, and preferably larger than about 10 microns. In the preferred embodiment, the length L may have a dimension of larger than about 1 micron, and preferably larger than about 5 microns. In the preferred embodiment, the area of the capacitor is greater than about 5 $\mu m^2$. The detailed structure of the capacitor may be seen in cross-sectional views along the lines A-A' and B-B' in Figures 8a and 8b.

**[0047]** The cross-sectional view along line A-A' is shown in Figure 8a. The top electrode 106 extends laterally into the isolation regions 116. The isolation regions 116 may comprise isolation structures known and used in the art, such as shallow trench isolation. The shallow trench isolation structure may comprise a dielectric filling material such as chemical vapor deposited silicon oxide. The shallow trench isolation structure 116 may also comprise trench liner oxide (not shown for simplicity) on the boundaries of the trench. The trench liner oxide may or may not contain nitrogen.

**[0048]** The top electrode in Figure 8a is shown to have a thickness t, preferably in the range of about 200 angstroms to about 2000 angstroms, typically less than about 500 angstroms. The capacitor structure 100 may additionally have spacers 134 formed on the sides of the top electrode 106. The top electrode 106 may be formed of the same material as the gate electrode of other transistors on the same chip.

**[0049]** The cross-sectional view along line B-B' is shown in Figure 8b. This figure shows that the bottom electrode 104 may be electrically connected via adjacent doped regions 110 and 112. In the case where the bottom electrode 104 is not heavily doped, the bottom electrode may

comprise an inversion layer 114. An inversion layer may be formed by a supply of mobile carriers from the adjacent doped regions 110 and 112, and when there is a substantial bias between the top and bottom electrodes. The substantial bias can be the potential between VDD and GND, between OVDD and GND, or between OVDD and VDD.

**[0050]** For reasons of simplicity, the contacts 140 have not been shown in the cross-sectional views of Figures 8a and 8b. These contact plugs 140 are shown in Figures 9a and 9b, which will be discussed next.

**[0051]** Figures 9a and 9b show yet another embodiment of the present invention where the strained silicon layer 104 is formed in a portion of the semiconductor substrate 102. In this case, the strain may be induced by local mechanical stress, such as that due to the influence of a high stress film 136. Figure 9a shows the cross-sectional view along line A-A' of Figure 7 and Figure 9b shows the cross-sectional view along line B-B' of Figure 7. These figures include the inter-layer dielectric 138 and contact plugs 140. Contact plugs 140 serve to electrically couple top electrode 106 (Figure 9a) and doped regions 110 and 112 (Figure 9b) to portions of the first metal layer 142. This metal layer 142 is covered by inter-layer dielectric 144.

**[0052]** The inter-layer dielectric (ILD) 138 and/or 144 can be a chemical vapor deposited dielectric such as silicon oxide. Either one or both of ILDs 138 and 144 can also be a low permittivity (low-k) dielectric employed in interconnect technology. For example, by using a low-k ILD 138 to cover the capacitor, parasitic capacitances between the top electrode 106 and metal lines 142 in the vicinity of the top electrode 106 can be reduced. By using a low-k ILD 144 over first metal layer 142, parasitic capacitances between the first metal layer 142 and the second metal layer (not shown) can also be reduced.

**[0053]** In the preferred embodiment, the relative permittivity of the low-k dielectric is less than about 3.5, and more preferably less than about 3.0. For example, the low-k dielectric material may be an organic material, such as benzocyclobutene (BCB), SILK™, FLARE™, or others. Alternatively, the low-k dielectric material may be an inorganic dielectric material, such as methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), SiOF, as examples. These materials are exemplary only as other embodiments may include different low-k dielectric materials.

**[0054]** A contact etch-stop layer 136 may overlie the top electrode 106 and the spacer 134, as shown in Figure 9a. The contact etch-stop layer 136 is preferably silicon nitride, but it is understood that other materials with a different etch rate from the ILD may be used. The silicon nitride etch-stop layer 106 may have an inherent stress in the range of –2 giga-pascals (GPa) to +2 GPa, where negative stress implies compressive stress and positive stress implies tensile stress.

**[0055]** As shown in Figure 9a, a contact plug 140 electrically couples the top electrode 106 to interconnect metal lines 142. As shown in Figure 9b, another contact plug 140 electrically connects the doped region 110 (112) in the semiconductor layer to the metal lines 142. This connection serves to electrically couple the bottom electrode 104 of the capacitor.

**[0056]** Next, a method of manufacturing the decoupling capacitor will be described with respect to Figures 10a-10f. Referring now to Figure 10a, a semiconductor substrate 102 comprising a topmost strained silicon layer 104 is provided. For example, the semiconductor substrate 102 may comprise a strained silicon layer overlying a relaxed SiGe layer as shown in Figure 3. The germanium concentration in the relaxed SiGe layer may be in the range of 10% to 90%, and more preferably from 20% to 40%. The thickness of the strained silicon layer 104 is

preferably below its critical thickness. In the preferred embodiment, the thickness of the strained silicon layer is in the range of about 20 angstroms to about 500 angstroms. In another example, the semiconductor substrate may be strained silicon on insulator substrate.

**[0057]** An active region mask 146 is used to define trenches 148 in the semiconductor layer 104. The mask 146 preferably comprises silicon nitride, and more preferably comprises silicon nitride on a silicon oxide layer. Trench filling dielectric material is deposited by chemical vapor deposition to fill the trenches to create isolation regions 116. As explained in co-pending application Serial No. 10/423,513 (TSM03-0173), the isolation regions 116 may induce additional stress. Application Serial No. 10/423,513 is incorporated herein by reference.

**[0058]** The process continues with a chemical mechanical process step to planarize the top surface of the device being fabricated. The mask 146 can then removed using common etching techniques. Figure 10b shows the cross-section at this stage in the fabrication process.

**[0059]** The bottom electrode 104 may or may not be heavily doped at this point. If an ion implantation step with a high dose is introduced into the active region 104 at this point to dope the semiconductor layer, a heavily doped bottom electrode can be formed. For example, the heavily doped active region or bottom electrode may have a doping concentration of larger than $10^{19}\,cm^{-3}$.

**[0060]** The capacitor dielectric 108 is then formed, as shown in Figure 10c. The physical thickness of the capacitor dielectric 108 may be smaller than 100 angstroms, more preferably smaller than 50 angstroms, and even more preferably smaller than 10 angstroms. The capacitor dielectric 108 may be formed together with the formation of a transistor gate dielectric in a different portion of the semiconductor chip (not shown). For example, the capacitor dielectric 108 may be formed by thermal oxidation, chemical vapor deposition, sputter deposition, or any

other techniques known and used in the art for forming gate dielectrics. By forming the capacitor dielectric together with the gate dielectric of a transistor in a different portion of the chip, no additional process steps are introduced. Dielectric materials as previously described may be used. The capacitor dielectric may be comprised of one or more layers of dielectric materials.

**[0061]** Referring to Figure 10d, the top electrode material 106 can then be deposited over the capacitor dielectric layer. The top electrode material 106 can be comprised of conventional poly-crystalline silicon, poly-crystalline silicon germanium, metals, metallic silicides, or metallic nitrides, as previously described. The top electrode material 106 may be deposited by conventional techniques such as chemical vapor deposition. The top electrode 106 may also be formed by the deposition of silicon and metal, followed by an anneal to form a metal silicide gate electrode material.

**[0062]** The top electrode material 106 is then patterned using photolithography techniques, and etched using plasma etch processes to form the gate electrodes. The deposition of the top electrode material may be the same process step as the deposition of gate electrode material of a transistor to be formed in a different portion of the semiconductor chip, and the etching of the top electrode may similarly be accomplished together with the etching of the gate electrode of the said transistor. The completed top electrode is shown in Figure 10d. The capacitor dielectric is retained at least in the portion of the capacitor covered by the top electrode.

**[0063]** At this point, doping may be introduced in regions adjacent to the bottom electrode to make electrical contacts with the bottom electrode. These regions are shown in the cross-section of Figure 8b and Figure 9b (in planes above and below the page in Figure 10d).

**[0064]** As shown in Figure 10e, spacers 134 may be additionally formed on the sides of the top electrode. This may be followed by another implant to dope the regions of the active region not covered by the spacers. Once again, these process steps follow the process used to form the lightly doped and heavily doped source and drain regions of the transistors (not shown) being fabricated on the chip.

**[0065]** A contact etch-stop layer 136 may be formed on the top electrode 106 and spacers 134. The etch-stop layer 136 may be a high-stress film such as a high-stress silicon nitride film deposited by plasma-enhanced chemical vapor deposition. The high-stress film may be used to enhance the strain in the strained silicon region 104.

**[0066]** An inter-layer dielectric (ILD) 138 may be formed over the capacitor and contact holes etched through the ILD 138 to reach the top and bottom electrodes of the capacitor. Conductive materials are then used to fill the contact holes to electrically contact the top and bottom electrodes. For example, a layer of tungsten can be formed to fill the holes and then either etched back or chemically-mechanically polished.

**[0067]** Although the capacitor described in this invention has been illustrated for use as a decoupling capacitance, it is understood that the capacitor thus formed according to this invention may be used for other purposes. For example, the capacitor may be used as a coupling capacitor. In another embodiment, the capacitor can be used as the storage cell in a dynamic random access memory or in a mixed signal circuit such as an analog-to-digital converter or a digital-to-analog converter.

**[0068]** While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention,

will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.